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Application Serial Number 10/783,817 Examiner Portka, Art Unit 2188

Proposed Amendment December 1, 2006

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It is Proposed the Claims be Amended as Follows:

- (Currently Amended) A main memory simulator for simulating large computer memories, wherein said large computer memories are defined by a plurality of target memory addresses, said simulator comprising:
- one or more mass storage devices having page addresses to simulate 4 said target memory addresses; 5
- 6 a memory cache; and
- a processor operable with said memory cache, wherein said processor 7 operates under instructions 8
- to move data contained in a predetermined range of more 9 frequently used target memory addresses between corresponding page addresses 10 in said mass storage devices and said memory cache on a fast memory access 11 basis, and 12
- to move data contained in a predetermined range of infrequently 13 less frequently used target memory addresses between corresponding page 14 addresses in said mass storage devices and said memory cache on a slow memory 15 access basis. 16
- (Currently Amended) The simulator of claim 1, wherein said fast memory access 1 2. comprises the utilization of a set of fast lookup tables to directly obtain a page address 2 that has been allocated to an address within the more frequently used range of target 3 4 memory addresses.
- (Currently Amended) The simulator of claim 1, wherein said slow memory access 1 3. comprises the utilization of a slow lookup table to first determine if a page address has 2 been allocated to an address within the infrequently less frequently used range of target 3
- memory addresses and to then obtain the allocated page address.

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- (Currently Amended) The simulator of claim 2, wherein sald slow memory access 1 comprises the utilization of a slow lookup table to determine if a page address has been 2 allocated to an address within the infrequently less frequently used range of target 3 memory addresses and the obtainment of said page address if allocated. 4
- (Original) The simulator of claim 1, wherein the movement of data is achieved 5. 1 2 through a page transfer.
- (Currently Amended) A main memory simulator for simulating large computer 1 6. memories, wherein said large computer memories are defined by a plurality of target 2 memory addresses, said simulator comprises: 3
- mass storage means for simulating said target memory addresses; 4
- means for storing data; 5
- means for processing instructions 6
- to transfer data. 7

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- said data being transferred between said mass storage means and said 8 9 means for storing
 - via a fast memory access scheme if said data resides within a predetermined range of more frequently accessed target memory addresses or
- via a slow memory access scheme if said data resides within a 12 predetermined range of infrequently less frequently addressed target memory 13 14 addresses.
- (Previously Amended) The simulator of claim 6, wherein said fast memory 1 access scheme comprises utilizing a set of fast lookup tables. 2

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- (Currently Amended) The simulator of claim 7, wherein said fast lookup tables 8. 1
- enable said means for processing to directly obtain a page address in said mass 2
- storage means corresponding to said data stored within said range of more frequently 3
- accessed target addresses. 4
- (Original) The simulator of claim 6, wherein said slow memory access scheme 1 9.
- comprises utilizing a slow lookup table. 2
- (Currently Amended) The simulator of claim 9, wherein said slow lookup table 10. 1
- enables said means for processing to first determine if a page address has been 2
- allocated to said data residing within said range of infrequently less frequently 3
- addressed memory addresses and then to obtain the allocated page address. 4
- (Original) The simulator of claim 6, wherein said transferring of data is achieved 11. 1
- through a page transfer. 2
- (Currently Amended) A method for simulating large computer memories via one 12. 1
- or more storage devices, wherein said large computer memories are defined by a 2
 - plurality of target memory addresses, and wherein said large computer memories are
- 3 large enough to prevent simulation via the use of one-to-one addressing for all of said 4
- plurality of memory addresses, the method comprising: 5
- obtaining a request for transfer of data residing within one of said target memory 6
- addresses if said data resides within a predetermined range of more frequently 7
- requested target memory addresses, then using a fast memory access scheme to do at 8
- least one of transferring the data to, and from, a corresponding address within said 9
- storage devices; and 10
- if the data resides within a predetermined range of infrequently less frequently 11
- requested target memory addresses, then using a slow memory access scheme to do 12

- 13 at least one of transferring the data to, and from, a corresponding address within said
- 14 storage devices.
- 1 13. (Original) The method of claim 12, wherein said fast memory access scheme
- 2 comprises utilizing a set of fast lookup tables.
- 1 14. (Currently Amended) The method of claim 13, wherein said fast lookup tables
- 2 enable direct obtainment of a page address in said storage devices corresponding to a
- 3 target memory address within said range of said more frequently accessed target
- 4 memory addresses.
- 1 15. (Original) The method of claim 12, wherein said slow memory access scheme
- 2 comprises utilizing a slow lookup table.
- 1 16. (Currently Amended) The method of claim 15, wherein said slow lookup table
- 2 first enables determining if a page address in said storage devices has been allocated
- 3 to a memory address within said range of infrequently less frequently addressed target
- 4 memory addresses that stores said data and then enables obtaining the allocated page
- 5 address.
- 1 17. (Original) The method of claim 12, wherein said transfer of data comprises a
- 2 page transfer.
- 1 18. (Currently Amended) A memory simulation system for simulating a main memory
- 2 of a computer, comprising:
- a plurality of files, wherein said files include a fast look-up table and a slow
- 4 look-up table,
- wherein said fast look-up table is operable to directly obtain a page address that
- 6 has been allocated to simulate a corresponding main memory address that is within at

- 7 least one of a predetermined range of <u>more</u> frequently accessed main memory
- 8 addresses, and
- wherein said slow look-up table is operable to obtain a page address that has
 been allocated to simulate a corresponding main memory address that is within at least
 one of a predetermined range of infrequently less frequently accessed main memory
 addresses;
- a cache; and
- an interface to receive a request for transfer of data residing at a requested main memory address, said transfer occurring between at least one of said plurality of files and said cache via use of one of said fast look-up table and said slow lookup table.
 - 1 19. (Previously Amended) The system of claim 18, wherein said plurality of files further include a last access look-up table, wherein said last access look-up table includes a last main memory address accessed and a page address allocated to said last main memory address accessed.
 - 20. (Currently Amended) The system of claim 18, wherein if said requested main memory address is within said at least one predetermined range of infrequently less frequently used addresses, a list of addresses simulating said main memory addresses is searched in attempt to locate a page address allocated to said requested main memory address, and if said page address is not located, allocating said page address for said requested main memory address.
- 1 21. (Original) The system of claim 18, wherein both said fast look-up table and said
- 2 slow look-up table are savable into a finite number of files.

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- 1 22. (Original) The system of claim 21, wherein said fast look-up table and said slow 2 look-up table are restorable from the saved files enabling a previously stopped
- 3 simulation to continue.
- 1 23. (Previously Amended) The system of claim 18, wherein said fast look-up table is
- 2 used to obtain a page address for any main memory address that resides within a
- 3 predetermined lowest address range within main memory address space.
- 1 24. (Currently Amended) The system of claim 23, wherein said fast look-up table is
- 2 divided into a plurality of banks, each bank having a defined number of words, and
- 3 wherein said requested main memory address is divided by said defined number of
- 4 words to obtain a quotient value, wherein said quotient value is compared against a
- 5 predetermined value to determine whether said requested main memory address is
- 6 within said at least one of said predetermined more frequently or said infrequently less
- 7 <u>frequently</u> accessed main memory address range.
 - 25. (Currently Amended) A memory simulation system for simulating main memory of a computer, the system comprising:

means for receiving a data transfer request to transfer data between one or more storage devices simulating said main memory, wherein said data transfer request is defined by a main memory address within said main memory;

means for determining the frequency of use of said main memory address based on which one of multiple pre-defined address ranges within said main memory contains said main memory address;

means for obtaining a page address corresponding to said main memory address, wherein said means for obtaining includes:

means for obtaining said page address corresponding to said main memory address when said main memory address has been determined to be more frequently used; and

- means for obtaining said page address corresponding to said main memory address when said main memory address has been determined to be infrequently less frequently used; and
- means for transferring data between said page address of one of said storage devices and an address within a different one of said storage devices.
- 1 26. (Currently Amended) The system of claim 25, wherein said means for obtaining
- the page address when said main memory address is more frequently used comprises
- 3 a set of fast lookup tables.
- 1 27. (Currently Amended) The system of claim 26, wherein said fast lookup tables
- 2 enable said means for obtaining to directly obtain the page address of the more
- 3 frequently used main memory address.
- 1 28. (Currently Amended) The system of claim 25, wherein said means for obtaining
- 2 the page address when said main memory address is infrequently less frequently used
- 3 comprises a slow lookup table.
- 1 29. (Original) The system of claim 28, wherein said slow lookup table enables said
- 2 means for obtaining to first determine if a page address has been allocated to said main
- 3 memory address and then to obtain that allocated pages address.
- 30. (Currently Amended) A method of memory transfer for use in simulating a main
- 2 memory the method comprising:
- 3 obtaining a main memory address, wherein said main memory address indicates a
- 4 request for a main memory transfer between a file simulating the main memory and a
- 5 cache buffer;

- determining, based on which of multiple pre-defined address ranges in said main
- 7 memory contains said main memory address, whether said main memory address
- 8 comprises memory that is accessed <u>more</u> frequently or <u>infrequently</u> <u>less frequently</u>;
- 9 if said main memory address comprises memory that is accessed more frequently,
- 10 directly obtaining a page address that has been allocated to said main memory address
- 11 through use of a first look-up table;
- 12 if said main memory address comprises memory that is accessed infrequently less
- 13 <u>frequently</u>, first determining whether a page address has been allocated to said main
- 14 memory address through use of a second lookup table, then obtaining the page address
- 15 that has been allocated to said main memory address;
- transferring data between said page address of said file and said cache buffer.
- 1 31. (Original) The method of claim 30, further comprising the step of saving the last
- 2 main memory address accessed and the corresponding page address.
- 1 32. (Currently Amended) The method of claim 30, wherein said second look-up table
- 2 contains a list of infrequently less frequently used ones of said main memory addresses
- 3 for which page addresses have been allocated.
- 1 33. (Original) The method of claim 30, further comprising the step of saving said first
- 2 look-up table and said second look-up table into a number of finite files.
- 1 34. (Original) The method of claim 33, further comprising the step of restoring said
- 2 first look-up table and said second look-up table to continue a previously stopped
- 3 simulation.

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- 1 35. (Currently Amended) The method of claim 30, wherein said first look-up table is
- divided into a plurality of banks, each bank having a defined number of words, and 2
- .3 wherein said step of determining is achieved by dividing said main memory address by
- said defined number of words to obtain a quotient value, then comparing said quotient 4
- value against a predetermined value, wherein the comparison provides an indication of 5
- whether said main memory address is more frequently or infrequently less frequently 6
- 7 addressed.